

IN THE CLAIMS

Please cancel claims 15-17, 22 and 23.

Please amend the claims as follows.

- 1 1. (Original) An apparatus comprising:
 - 2 at least one processor;
 - 3 a memory coupled to the at least one processor;
 - 4 an integrated circuit design residing in the memory, the integrated circuit design
 - 5 including a plurality of logic blocks;
 - 6 a static timing tool residing in the memory and executed by the at least one
 - 7 processor, the static timing tool performing analysis that results in a plurality of slack
 - 8 computations;
 - 9 a timing analysis mechanism residing in the memory and executed by the at least
 - 10 one processor, the timing analysis mechanism allowing a user to identify in the integrated
 - 11 circuit design at least one common logic block through which a clock test signal and a
 - 12 data launch signal both pass resulting in the clock test signal and data launch signal
 - 13 occurring on opposite edges at a subsequent logic block, the timing analysis mechanism
 - 14 improving at least one of the plurality of slack computations due to the at least one
 - 15 common logic block.
- 1 2. (Original) The apparatus of claim 1 wherein the static timing tool is EinsTimer.
- 1 3. (Original) The apparatus of claim 1 wherein the timing analysis mechanism
 - 2 determines a difference between fastest and slowest delay through the user-identified at
 - 3 least one common logic block, multiplies the difference by a correction factor, and adjusts
 - 4 the slack by the difference multiplied by the correction factor.

1 4. (Original) The apparatus of claim 1 wherein the timing analysis mechanism improves
2 at least one of the plurality of slack computations using at least one user delta adjust
3 parameter to adjust the clock test signal.

1 5. (Original) The apparatus of claim 1 wherein the timing analysis mechanism provides
2 input to the static timing tool but is not part of the static timing tool.

1 6. (Original) An apparatus comprising:
2 at least one processor;
3 a memory coupled to the at least one processor;
4 an integrated circuit design residing in the memory, the integrated circuit design
5 including a plurality of logic blocks;
6 a static timing tool residing in the memory and executed by the at least one
7 processor, the static timing tool performing analysis that results in a plurality of slack
8 computations; and
9 a timing analysis mechanism residing in the memory and executed by the at least
10 one processor, the timing analysis mechanism being separate from the static timing tool
11 and providing input to the static timing tool, the timing analysis mechanism allowing a
12 user to identify at least one common logic block through which a clock test signal and a
13 data launch signal both pass resulting in the clock test signal and the data launch signal
14 occurring on opposite edges at a subsequent logic block, the timing analysis mechanism
15 improving at least one of the plurality of slack computations due to the at least one
16 common logic block using at least one user delta adjust parameter to adjust the clock test
17 signal.

1 7. (Original) The apparatus of claim 6 wherein the static timing tool is EinsTimer.

1 8. (Original) The apparatus of claim 6 wherein the timing analysis mechanism
2 determines a difference between fastest and slowest delay through the user-identified at
3 least one common logic block, multiplies the difference by a correction factor, and adjusts
4 the slack by the difference multiplied by the correction factor.

1 9. (Original) A computer-implemented method for performing static timing analysis on
2 an integrated circuit design, the method comprising the steps of:
3 identifying a first logic block in the integrated circuit design that includes a clock
4 test signal and a data launch signal that occur on opposite edges;
5 calculating slack between the clock test signal and the data launch signal;
6 allowing a user to identify at least one common block through which both the
7 clock test signal and the data launch signal pass before reaching the first logic block; and
8 adjusting the slack according to delay characteristics through the at least one
9 common block.

1 10. (Original) The method of claim 9 wherein the step of adjusting the slack comprises
2 the steps of:
3 (A) determining a difference between fastest and slowest delay through the user-
4 identified at least one common block;
5 (B) multiplying the difference in (A) by a correction factor; and
6 (C) adjusting the slack by the result of the calculation in (B).

1 11. (Original) A computer-implemented method for performing static timing analysis on
2 an integrated circuit design, the method comprising the steps of:
3 identifying a first logic block in the integrated circuit design that includes a first
4 clock test signal and data launched by a first data launch signal, where the first clock test
5 signal and the first data launch signal occur on the same edge;
6 calculating a first slack number corresponding to slack between the first clock test
7 signal and the data launched by the first data launch signal;
8 automatically identifying a first set of common blocks through which both the
9 first clock test signal and the first data launch signal pass before reaching the first logic
10 block;
11 automatically adjusting the first slack number according to delay characteristics
12 through the first set of common blocks;
13 identifying a second logic block in the integrated circuit design that includes a
14 second clock test signal and data launched by a second data launch signal where the
15 second clock test signal and the second data launch signal occur on opposite edges;
16 calculating a second slack number corresponding to slack between the second
17 clock test signal and the data launched by the second data launch signal;
18 allowing a user to identify a second set of common blocks through which both the
19 second clock test signal and the second data launch signal pass before reaching the second
20 logic block; and
21 adjusting the second slack number according to delay characteristics through the
22 second set of common blocks.

1 12. (Currently Amended) The method of claim 11 wherein the step of adjusting the
2 second slack number comprises the steps of:
3 (A) determining a difference between fastest and slowest delay through the user-
4 identified ~~at least one common block~~ second set of common blocks;
5 (B) multiplying the difference in (A) by a correction factor; and
6 (C) adjusting the slack by the result of the calculation in (B).

1 13. (Original) The method of claim 11 wherein the step of adjusting the second slack
2 number comprises the step of defining at least one user delta adjust parameter for the
3 second clock test signal.

1 14. (Currently Amended) A computer readable program product comprising:
2 a timing analysis mechanism that allows a user to identify in an integrated circuit
3 design at least one common logic block through which a clock test signal and a data
4 launch signal both pass when the clock test signal and data launch signal occur on
5 opposite edges at a subsequent logic block, the timing analysis mechanism improving at
6 least one of a plurality of slack computations due to the at least one common logic block;
7 and
8 ~~computer readable signal bearing~~ recordable media bearing the timing analysis
9 mechanism.

1 15. (Cancelled)

1 16. (Cancelled)

1 17. (Cancelled)

1 18. (Original) The program product of claim 14 wherein the timing analysis mechanism
2 determines a difference between fastest and slowest delay through the user-identified at
3 least one common logic block, multiplies the difference by a correction factor, and adjusts
4 the slack by the difference multiplied by the correction factor.

1 19. (Original) The program product of claim 14 wherein the timing analysis mechanism
2 improves at least one of the plurality of slack computations using at least one user delta
3 adjust parameter to adjust the clock test signal.

1 20. (Currently Amended) The program product of claim 14 wherein the timing analysis
2 mechanism provides input to ~~[[the]]~~ a static timing tool but is not part of the static timing
3 tool.

1 21. (Currently Amended) A computer readable program product comprising:
2 a timing analysis mechanism that is separate from a static timing tool and that
3 provides input to the static timing tool, the timing analysis mechanism allowing a user to
4 identify at least one common logic block through which a clock test signal and a data
5 launch signal both pass when the clock test signal and data launch signal occur on
6 opposite edges at a subsequent logic block, the timing analysis mechanism improving at
7 least one of [[the]] a plurality of slack computations due to the at least one common logic
8 block using at least one user delta adjust parameter to adjust the clock test signal; and
9 ~~computer readable signal bearing~~ recordable media bearing the timing analysis
10 mechanism.

1 22. (Cancelled)

1 23. (Cancelled)

1 24. (Original) The program product of claim 21 wherein the static timing tool is
2 EinsTimer.

1 25. (Currently Amended) The program product of claim 21 wherein the timing analysis
2 mechanism determines a difference between fastest and slowest delay through the user-
3 identified at least one common logic block, multiplies the difference by a correction
4 factor, and adjusts the at least one slack computation by the difference multiplied by the
5 correction factor.